AMENDMENTS TO THE CLAIMS:

Kindly amend claims as follows:

1. (currently amended) A rate n/n recursive, ~~systematic~~ convolutional encoder which comprises:

n inputs, wherein n is an integer greater than 1;

n parallel outputs;

an adder having (n+1) inputs and an output; and

a feedback loop, including one or more storage elements in series, coupled to the output of the adder and to an input thereof, the feedback loop and the one or more storage elements being characterized by a ~~prime~~ polynomial that is prime relative to a predetermined field under which the arithmetic used to implement the encoder operates;

wherein all n encoder inputs are input to the adder, (n-1) of the encoder inputs are passed through unaltered to form (n-1) of the encoder outputs, and the nth encoder output is derived from the feedback loop.

2. (original) The encoder of claim 1 wherein the feedback loop includes a single storage element having an input and an output, wherein the input of the storage element is coupled to the output of the adder, and the output of the storage element is coupled to an input of the adder, and the nth encoder output is derived from the output of the storage element.

3. (canceled)

4. (original) The encoder of claim 1 in which n is 2.

5. (original) The encoder of claim 1 in which n is 3.

6. (original) The encoder of claim 1 in which n is 4.

7. (original) The encoder of claim 1 in which n is 5.

8. (original) The encoder of claim 1 in which n is 6 or greater.

9. (original) The encoder of claim 1 in combination with a D-dimensional bit to symbol mapper, wherein D is an integer greater than or equal to 1.

10. (original) The combination of claim 9 in which the mapper is a Gray mapper.

11. (original) The combination of claim 10 in which the encoder is a rate 3/3 encoder, and the mapper maps each 3-tuple output from the encoder into an 8-PSK symbol.

12. (original) The combination of claim 10 in which the encoder is a rate 6/6 encoder, and the mapper is a four-dimensional mapper which maps each of the two 3-tuples derived from a 6-tuple output from the encoder into an 8-PSK symbol having I and Q (quadrature) components.

13. (original) The combination of claim 10 in which the encoder is a rate 4/4 encoder, and the mapper maps each 4-tuple output from the encoder into a 16-QAM symbol.

14. (original) The combination of claim 10 in which the encoder is a rate 8/8 encoder, and the mapper is a four-dimensional mapper which maps each of the 4-tuples derived from the 8-tuple output from the encoder into a 16-QAM symbol.

15. (original) The combination of claim 10 in which the encoder is a 12/12 encoder, and the mapper is a six-dimensional mapper which maps each of the 4-tuples derived from the 12-tuple output from the encoder into a 16-QAM symbol.

16. (original) The combination of claim 10 in which the encoder is a rate 8/8 encoder, and the mapper maps each 8-tuple output from the encoder into a 256-QAM symbol.

17. (original) The combination of claim 10 in which the encoder is a rate 12/12 encoder, and the mapper is a four-dimensional mapper which maps each of the 6-tuples derived from the 12-tuple output into a 64-QAM symbol.

18. (original) The combination of claim 10 in which the encoder is a rate 12/12 encoder, and the mapper maps each of the 12-tuples output from the encoder into a 4096-QAM symbol.

19. (original) The combination of claim 9 in which D is greater than or equal to 2 and a multiplexor is coupled to the output of the mapper for serializing the D components of each channel symbol.

20. (currently amended) ~~An~~ A serial concatenated trellis coded modulation (SCTCM) encoder which includes the combination of claim 9 as its inner encoder.

21. (currently amended) ~~An~~ A serial concatenated trellis coded modulation (SCTCM) encoder which includes the combination of claim 19 as its inner encoder.

22. (currently amended) A~~n~~ serial concatenated convolutional code (SCCC) encoder which includes the encoder of claim 1 as its inner encoder.

23. (original) A transmitter which includes the SCTCM encoder of any of claims 20 or 21.

24. (original) A transmitter which includes the SCCC encoder of claim 22.

25. (original) A transceiver which includes the transmitter of any of claims 23 or 24.

26. (original) The transceiver of claim 25 which is a satellite transceiver.

27. (original) The transceiver of claim 25 which is a wireless transceiver.

28. (original) The transceiver of claim 25 which is a wireline transceiver.

29. (original) A wireless device which includes the transceiver of any of claims 26 or 27.

30. (original) The wireless device of claim 29 which is a mobile wireless device.

31. (currently amended) A method of performing TCM modulation comprising the steps of:

providing an n-tuple of bits, wherein n is an integer greater than 1, as an input to an inner encoder comprising a ~~the~~ rate n/n encoder comprising n inputs, n parallel outputs, an adder having (n+1) inputs and an output, and a feedback loop, including one or more storage elements in series, coupled to the output of the adder and to an input thereof, the feedback loop and the one or more storage elements being characterized by a polynomial that is prime relative to a predetermined field under which the arithmetic used to implement the encoder operates, wherein all n encoder inputs are input to the adder, (n-1) of the encoder inputs are passed through unaltered to form (n-1) of the encoder outputs, and the nth encoder output is derived from the feedback loop~~of claim 1, wherein n is an integer greater than 1~~;

receiving an n-tuple of bits as an output from the inner encoder; and

mapping the n-tuple of output bits into a D-dimensional channel symbol, wherein D is an integer greater than or equal to 1.

32. (original) The method of claim 31 wherein the mapping step employs Gray mapping.

33. (original) The method of claim 31 wherein D=1.

34. (original) The method of claim 31 wherein D>1.

35. (original) The method of claim 34 further comprising serializing the D components of the channel symbol.

36. (original) The combination of claim 10 in which the encoder is a rate 2/2 encoder, and the mapper maps each 2-tuple output from the encoder into two QPSK symbols.

37. (original) The combination of claim 10 in which the encoder is a rate 4/4 encoder, and the mapper maps each of the two 2-tuples derived from the 4-tuple output from the encoder into a QPSK symbol having I and Q components.

38. (currently amended) A method of performing TCM modulation comprising the following steps:

providing a k-tuple of bits as an input to an outer encoder comprising a convolutional encoder having redundancy, the outer encoder producing an n-tuple of bits, where both n and k are integers and n>k;

passing the n-tuple of bits through an interleaver, which outputs an n-tuple of interleaved bits;

providing the n-tuple of interleaved bits as input to an inner encoder comprising ~~the~~ a rate n/n encoder comprising n inputs, wherein n is an integer greater than 1, n parallel outputs, an adder having (n+1) inputs and an output, and a feedback loop, including one or more storage elements in series, coupled to the output of the adder and to an input thereof, the feedback loop and the one or more storage elements being characterized by a polynomial that is prime relative to a predetermined field under which the arithmetic used to implement the encoder operates, wherein all n encoder inputs are input to the adder, (n-1) of the encoder inputs are passed through unaltered to form (n-1) of the encoder outputs, and the nth encoder output is derived from the feedback loop ~~of claim 1~~;

receiving an n-tuple of output bits from the inner encoder; and

mapping the n-tuple of output bits into a D-dimensional channel symbol, where D is an integer greater than or equal to 1.

39. (currently amended) A method of performing SCC modulation comprising the following steps:

providing a k-tuple of bits as an input to an outer encoder comprising a convolutional encoder having redundancy, the outer encoder producing an n-tuple of bits, where both n and k are integers and n>k;

passing the n-tuple of bits through an interleaver, which outputs an n-tuple of interleaved bits;

providing the n-tuple of interleaved bits as input to an inner encoder comprising ~~the~~ a rate n/n encoder comprising n inputs, wherein n is an integer greater than 1, n parallel outputs, an adder having (n+1) inputs and an output, and a feedback loop, including one or more storage elements in series, coupled to the output of the adder and to an input thereof, the feedback loop and the one or more storage elements being characterized by a polynomial that is prime relative to a predetermined field under which the arithmetic used to implement the encoder operates, wherein all n encoder inputs are input to the adder, (n-1) of the encoder inputs are passed through unaltered to form (n-1) of the encoder outputs, and the nth encoder output is derived from the feedback loop ~~of claim 1~~;

receiving an n-tuple of output bits from the inner encoder; and

mapping the n-tuple of output bits into a QPSK or BPSK channel symbol.

40. (original) A method of decoding channel symbols comprising the steps of:

receiving channel symbols as produced by the method of any of claims 38 or 39 after transmission over a channel;

providing the channel symbols through an inner decoder which receives first a prior information and produces first a posteriori information from the channel symbols and the first a priori information;

passing the first a posteriori information through a de-interleaver to produce second a priori information for an outer decoder;

inputting the second a priori information to the outer decoder which produces second a posteriori information;

passing the second a posteriori information from the outer decoder through an interleaver to produce the first a priori information input to the inner decoder;

iterating through the foregoing steps a prescribed number p of iterations, where p is an integer greater than or equal to 1; and

after the prescribed number p of iterations, forming estimates of source bits from third a posteriori information provided by the outer decoder.

41. (currently amended) A serial concatenated trellis coded modulation (SCTCM) decoder embodying the method steps of claim 40.

42. (currently amended) A serial concatenated convolutional code (SCCC) decoder embodying the method steps of claim 39.

43. (currently amended) A system which comprises a transmitter including ~~the~~ an SCTCM encoder ~~of any of claims 20 or 21~~, and one or more receivers each including the SCTCM decoder of claim 41, the transmitter configured to broadcast information to the one or more receivers over a transmission link.

44. (original) The system of claim 43 wherein the link is a wireless link.

45. (original) The system of claim 43 wherein the link is a wireline link.

46. (original) The system of claim 43 wherein the link is a satellite link.

47. (currently amended) A system which comprises a transmitter including ~~the~~ a serial concatenated convolutional code (SCCC) encoder ~~of claim 22,~~ and one or more receivers each including the SCCC decoder of claim 42, the transmitter configured to broadcast information to the one or more receivers over a transmission link.

48. (original) The combination of claim 10 in which the encoder is a rate 10/10 encoder, and the mapper is a two-dimensional mapper which maps each 10-tuple output from the encoder into a 1024-QAM channel symbol.

49. (original) The combination of claim 10 in which the encoder is a rate 20/20 encoder, and the mapper is a four-dimensional mapper which maps each of the 10-tuples derived from a 20-tuple output from the encoder into a 1024-QAM channel symbol.

50. (original) The combination of claim 10 in which the encoder is a rate 60/60 encoder, and the mapper is a six-dimensional mapper which maps each of the 10-tuples derived from a 60-tuple output from the encoder into a 1024-QAM symbol.

51. (original) The combination of claim 10 in which the encoder is a rate 9/9 encoder, and the mapper is a six-dimensional mapper which maps each of the three-tuples derived from a 9-tuple output from the encoder into an 8-PSK channel symbol.

AMENDMENTS TO THE DRAWINGS:

Amendments to the drawings are reflected in Replacement Sheets and Annotated Sheets Showing Changes, which are attached to this paper following page 21. Kindly allow the following amendments to the drawings:

Figure 1A has been amended by adding legend "prior art," by labeling reference block 3, and by removing arrows from reference numeral indicators 1, 2 and 5.

Figure 1B has been amended by adding legend "prior art" and by removing arrows from reference numeral indicators 6 and 10.

Figure 1C has been amended by adding legend "prior art," by removing arrows from reference numeral indicators 11 and 18, and by exchanging locations of outputs 15 and 18.

Figure 3A has been amended by labeling reference block 25, by deleting reference numerals 23a and 23b, and by removing arrows from reference numeral indicators 21a, 21b, 21c, 22a, 22b, 22c, and 24.

Figure 3B has been amended by labeling reference block 31, by deleting reference numerals 29a and 29b, and by removing arrows from reference numeral indicators 27a, 27b, 27c, 28, 30a, 30b, 30c, 32, and 33.

Figure 4 has been amended by labeling reference block 37 and by removing arrows from reference numeral indicators 34a, 34b, 35a, 35b, and 36.

Figure 5 has been amended by labeling reference block 42, by deleting reference numerals 41a, 41b, and 41c, and by removing arrows from reference numeral indicators 39a, 39b, 39c, 39d, 40a, 40b, 40c, 40d, and 63. Also, the connector from 39a to 63 has been replaced with a connector from 39b to 63.

Figure 6 has been amended by replacing the term "m inputs" with the term "D components," and by removing arrows from reference numeral indicators 48 and 49.

Figures 7A, 8A, and 9A have each been amended by labeling the reference block.

Figures 9B, 10, and 16 have each been amended by centering on the drawing sheet.

Figure 11A has been amended by labeling reference blocks 61a, 61b, and 61c, and by removing arrows from reference numeral indicators 58, 62, 63b, and 63c. Also, the brackets for reference numerals 55 and 60 have been resized.

Figure 11B has been amended by labeling reference block 61, and by removing arrows from reference numeral indicators 58 and 62.

Figure 15 has been amended by removing reference numeral 200.

Figure 17 has been amended by renumbering the process blocks consecutively from 126 to 134, and by resizing the blocks and type font.